

Board 1 of 2

Board 1 of 2

Board 2 of 2

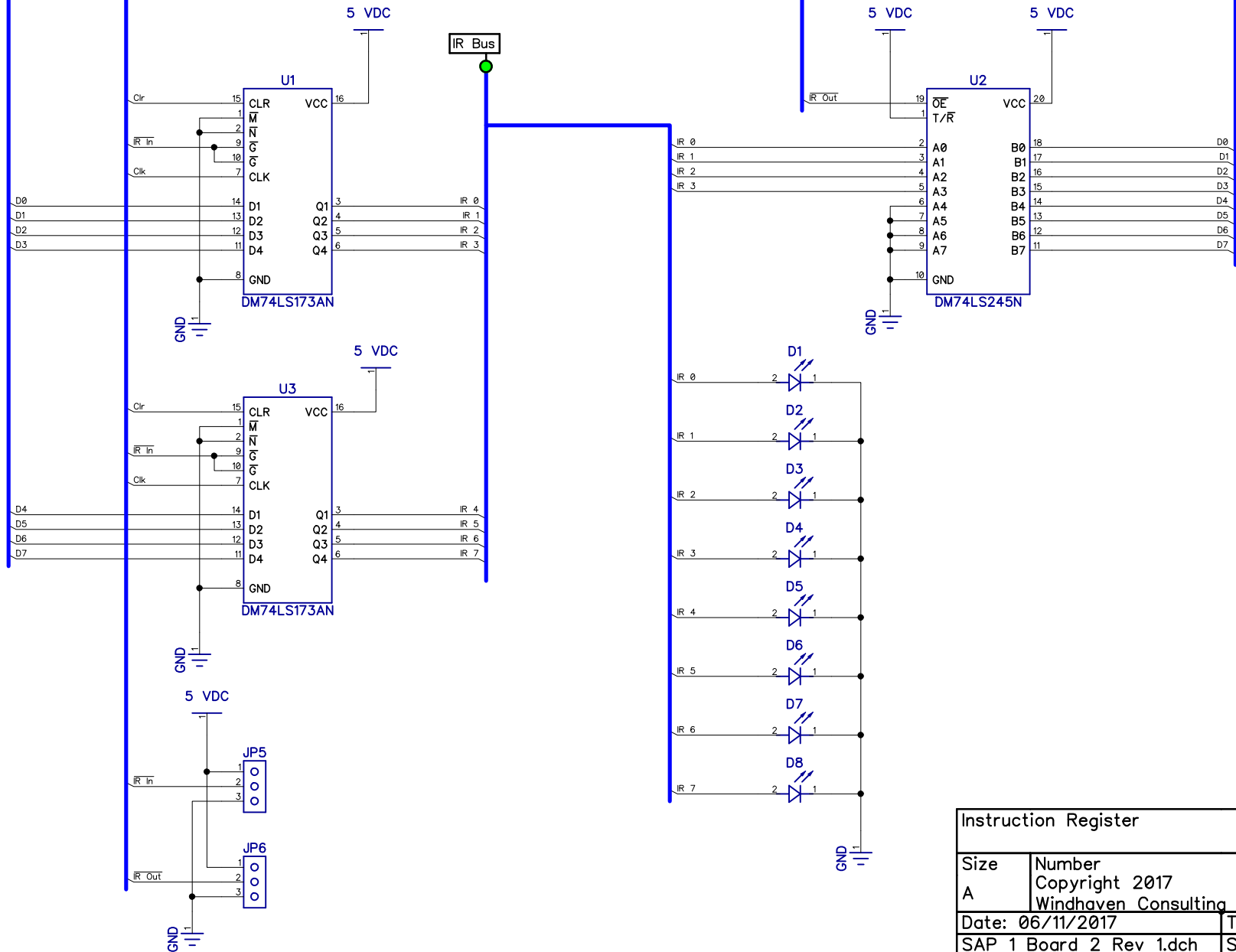
Board 2 of 2

SAP 1 Computer Block Diagram		
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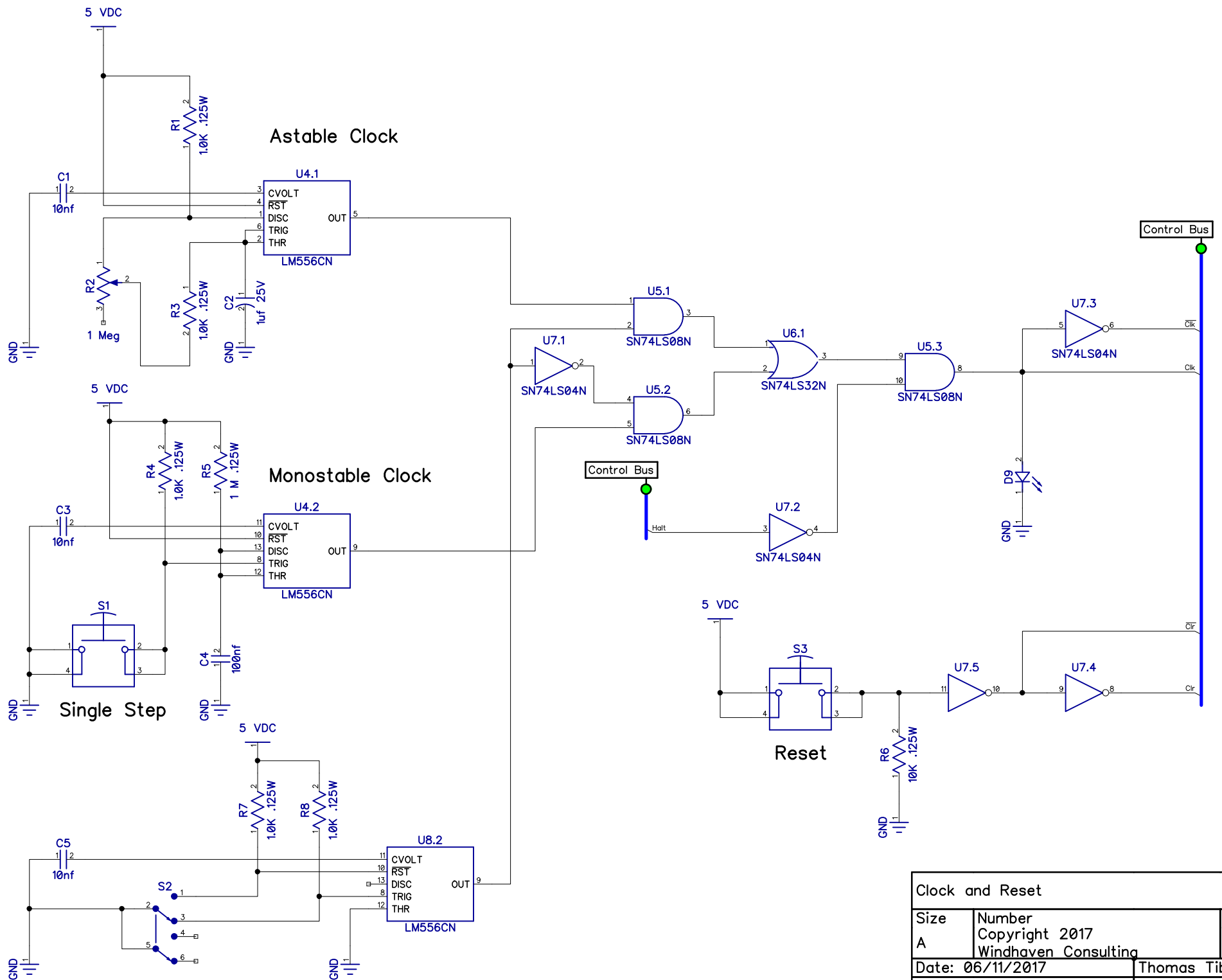
W Bus

Control Bus

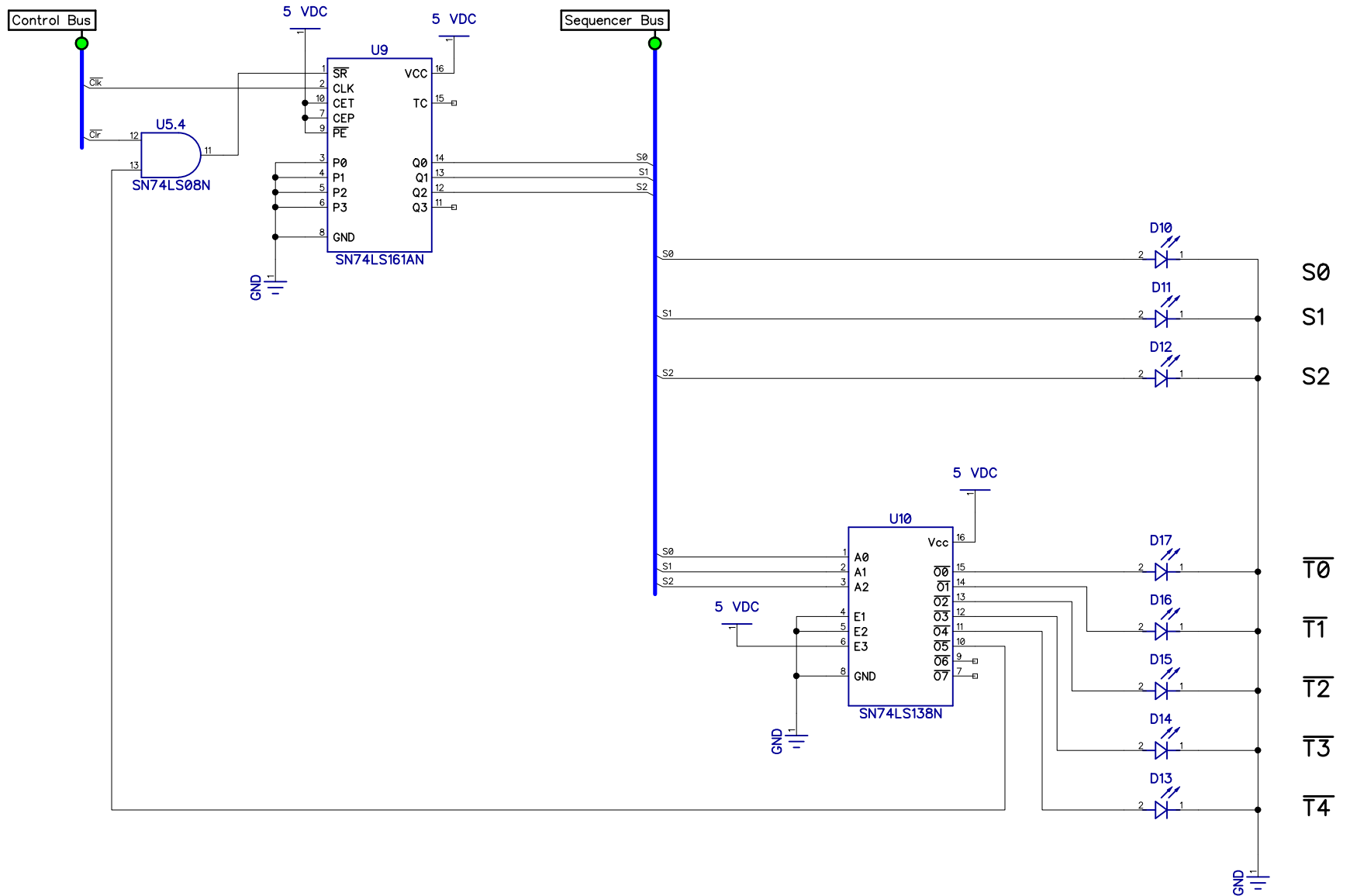
IR Bus



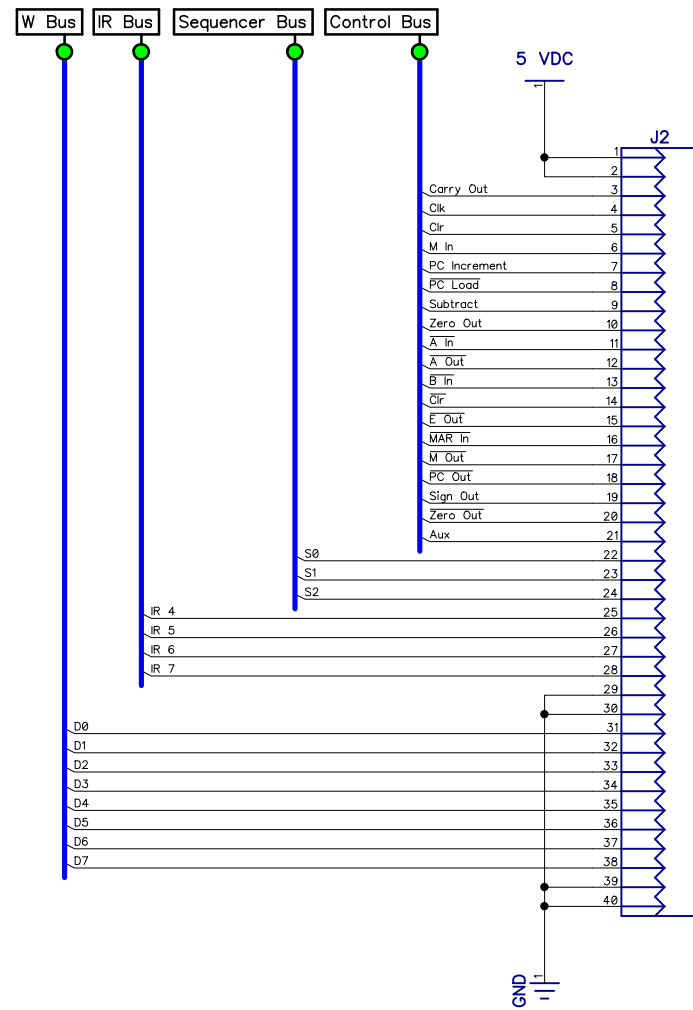
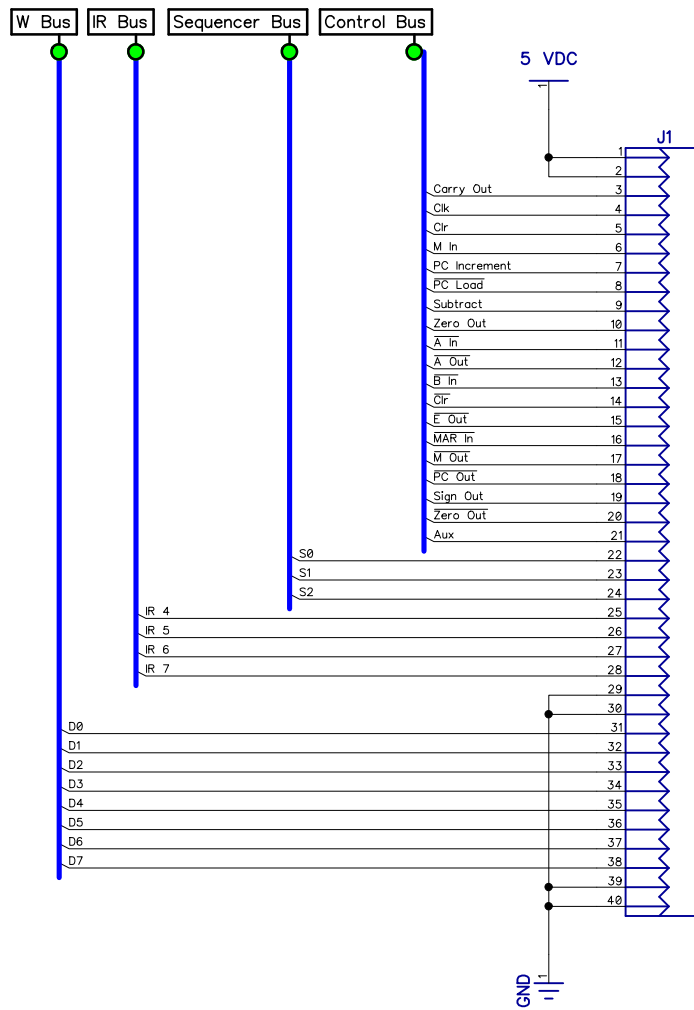
Instruction Register		
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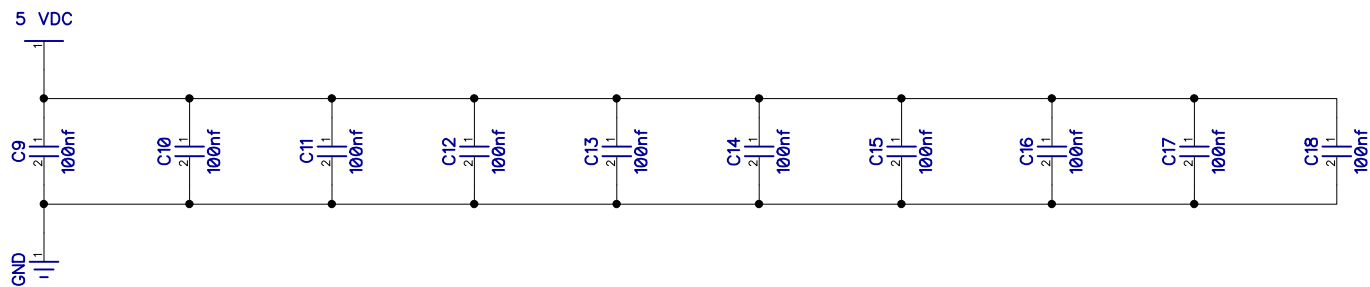
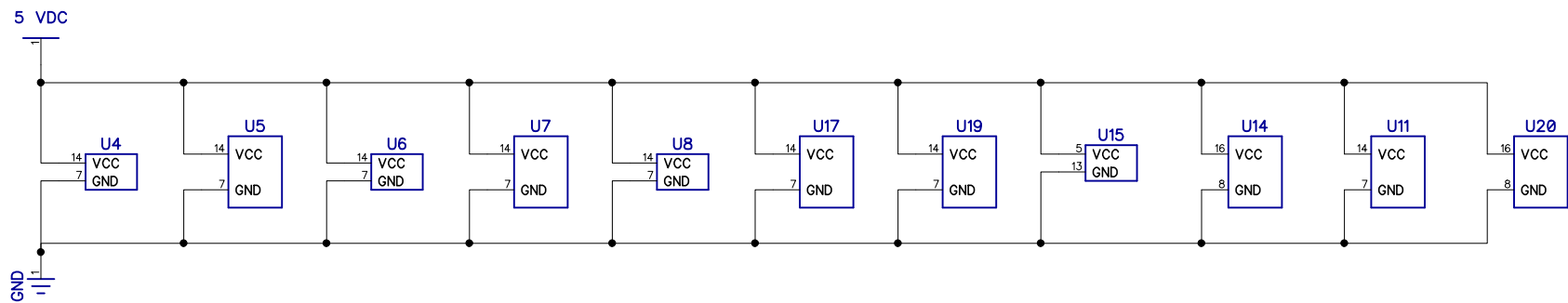
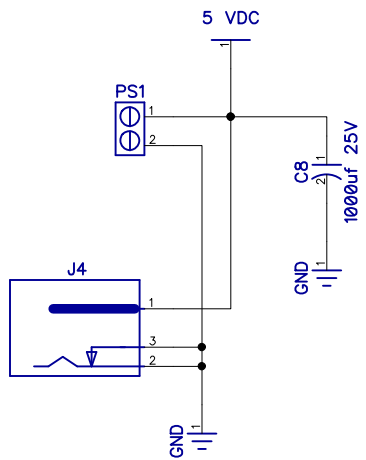
Clock and Reset		
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Timing and Sequence		
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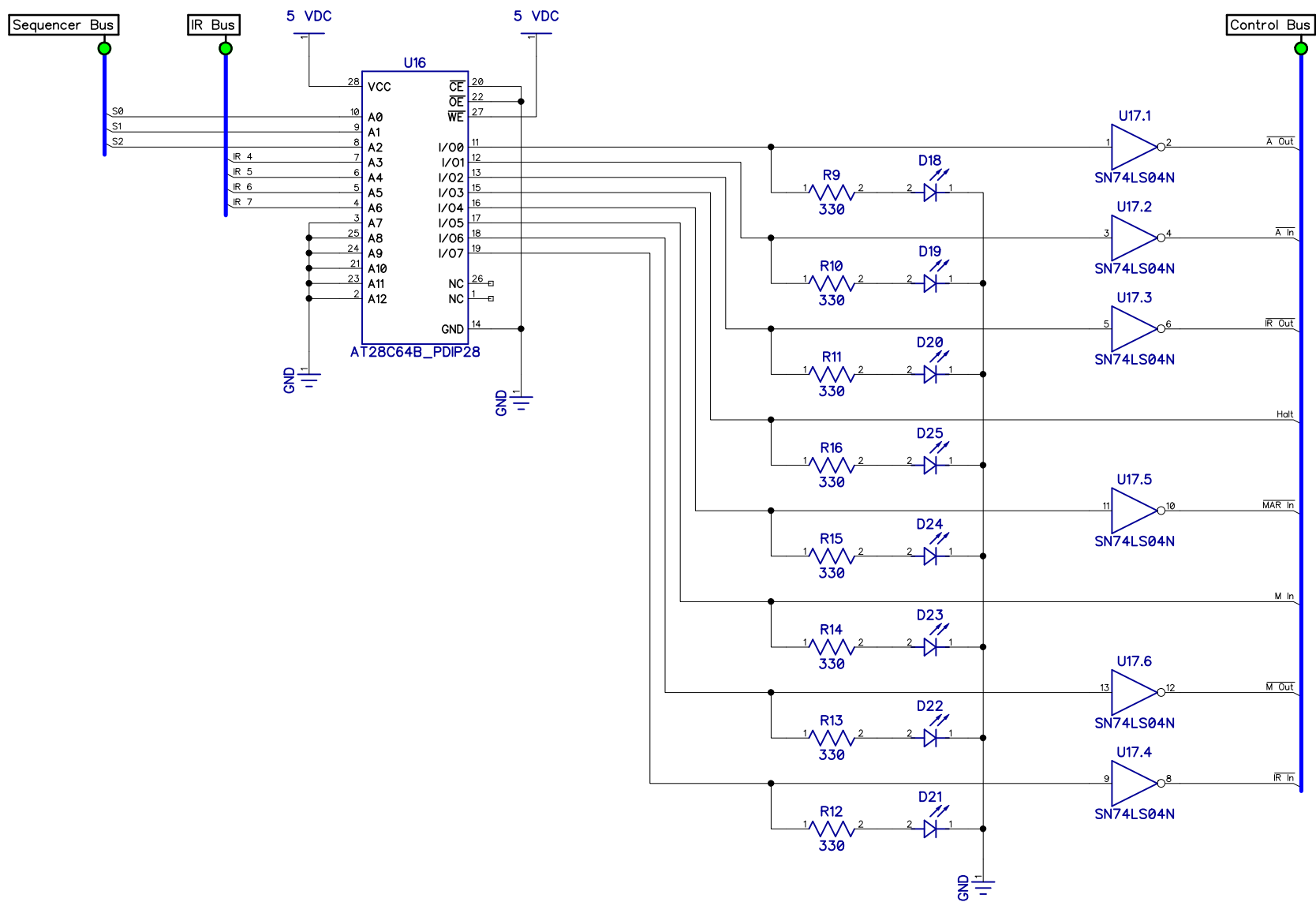


External Interface		
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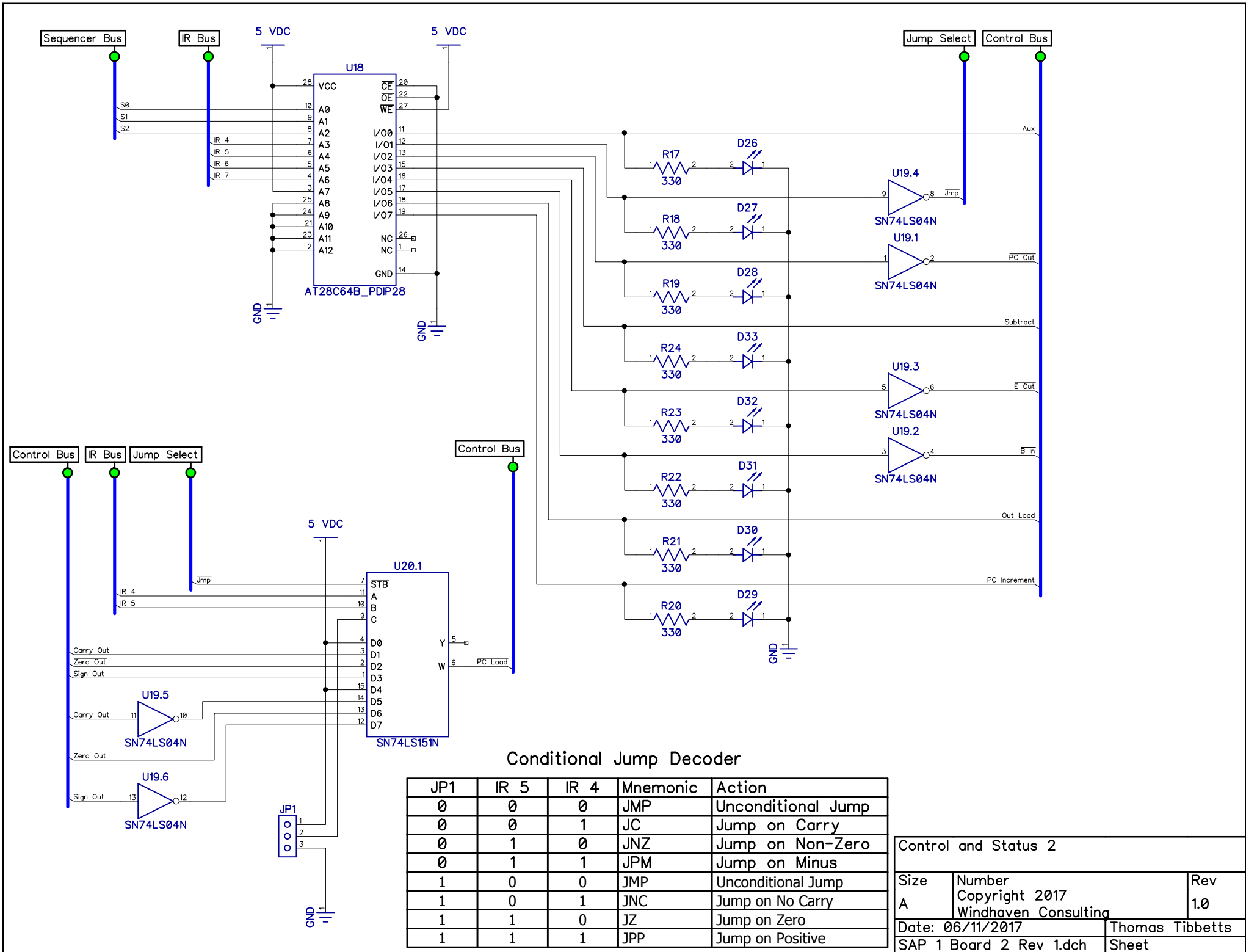
Power Distribution		
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Control and Status 1		
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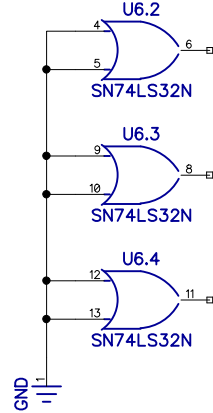
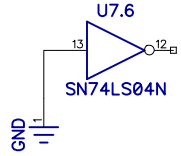
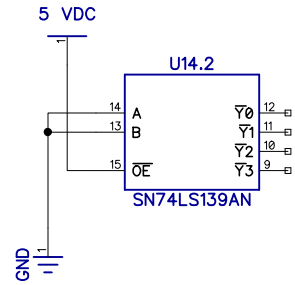
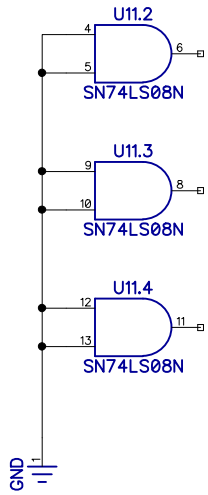




Conditional Jump Decoder

JP1	IR 5	IR 4	Mnemonic	Action
0	0	0	JMP	Unconditional Jump
0	0	1	JC	Jump on Carry
0	1	0	JNZ	Jump on Non-Zero
0	1	1	JPM	Jump on Minus
1	0	0	JMP	Unconditional Jump
1	0	1	JNC	Jump on No Carry
1	1	0	JZ	Jump on Zero
1	1	1	JPP	Jump on Positive

Control and Status 2		
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Spares		
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